FIG. 1

PRIOR ART

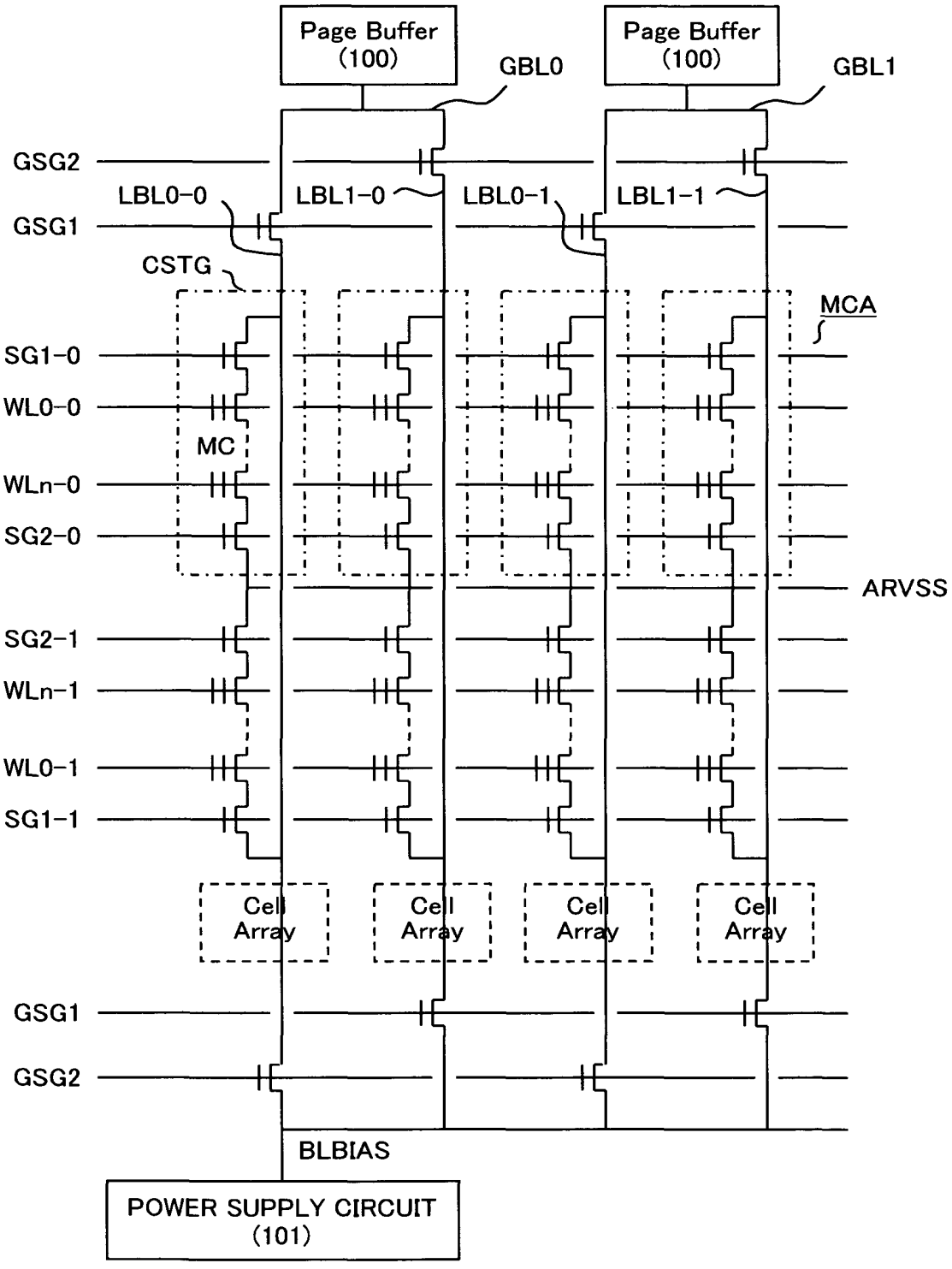


FIG. 2

PAGE BUFFER 100

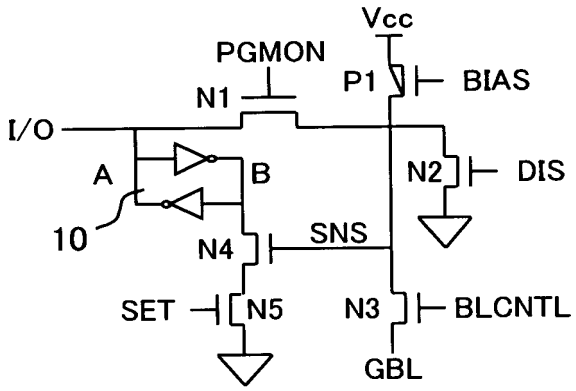


FIG. 3

POWER SUPPLY CIRCUIT 101

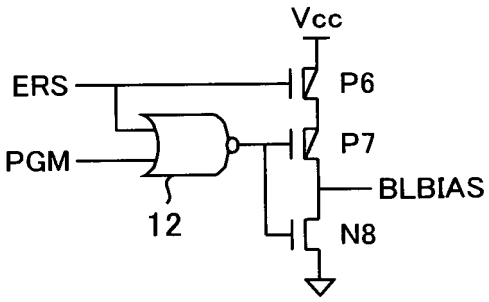


FIG. 4

AC SENSE FOR READ OPERATION OF PRIOR ART

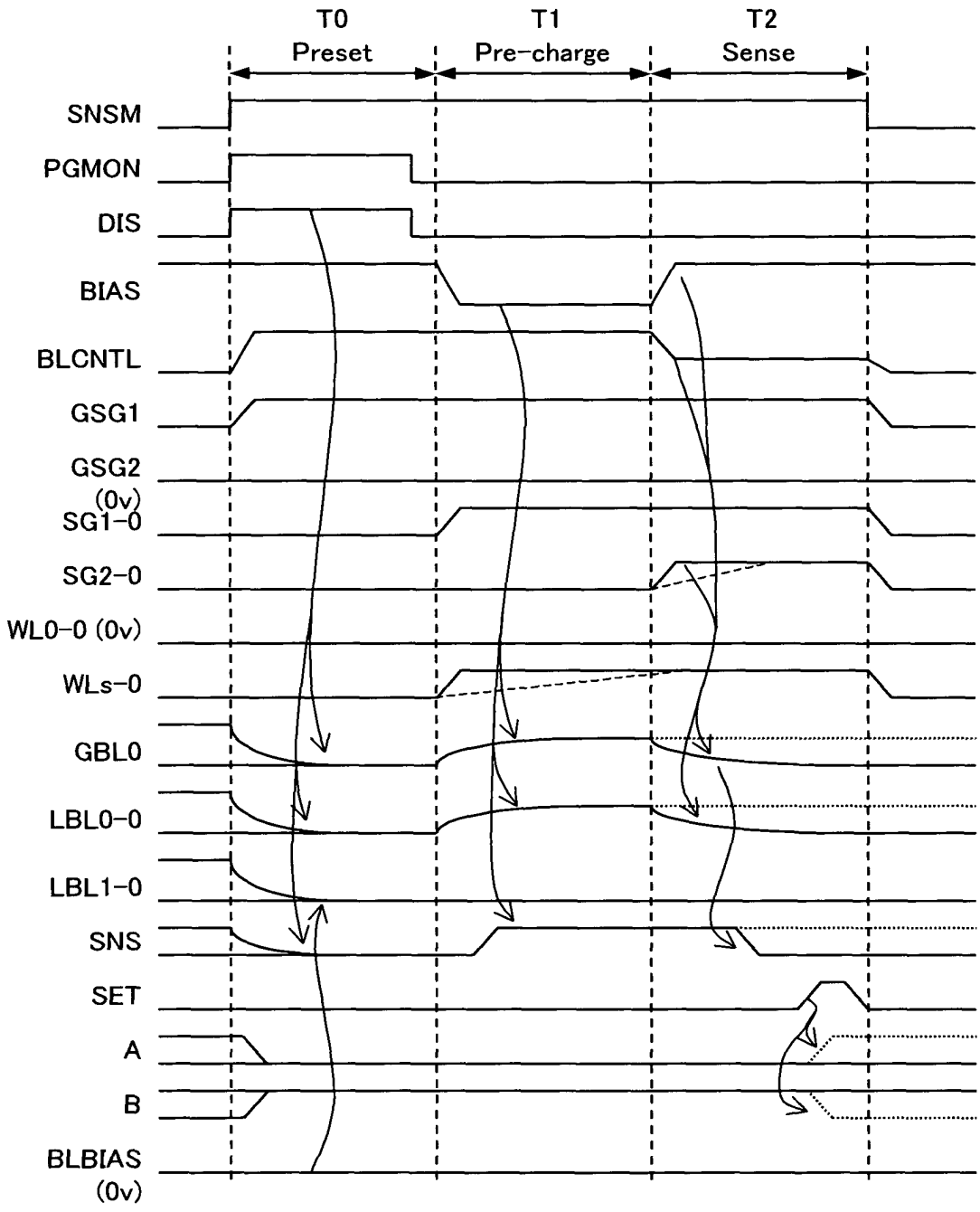


FIG. 5

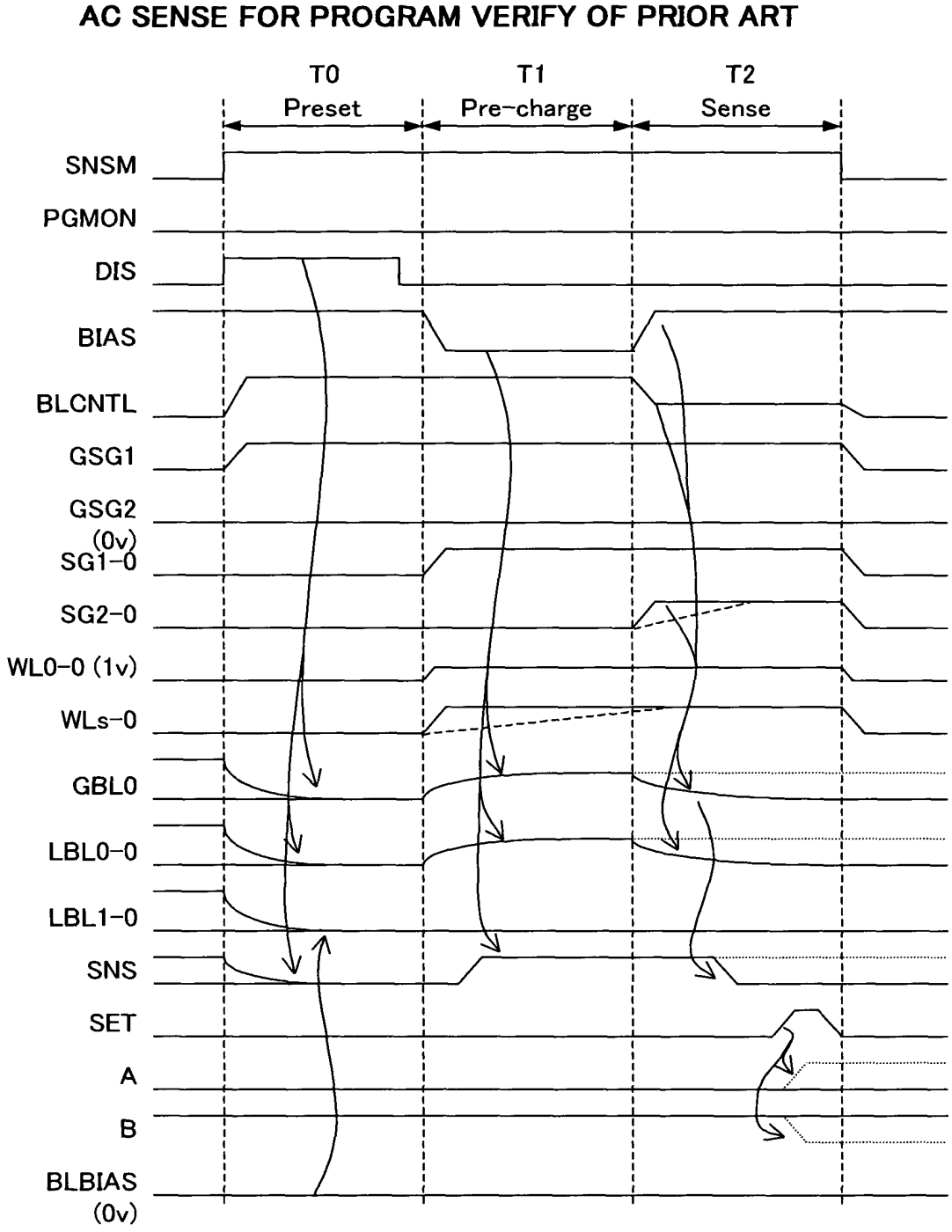

AC SENSE FOR PROGRAM VERIFY OF PRIOR ART
T0
Preset
T1
Pre-charge
T2
Sense
SNSM
PGMON
DIS
BIAS
BLCNTL
GSG1
GSG2
(0v)
SG1-0
SG2-0
WL0-0 (1v)
WLs-0
GBL0
LBL0-0
LBL1-0
SNS
SET
A
B
BLBIAS
(0v)

FIG. 6

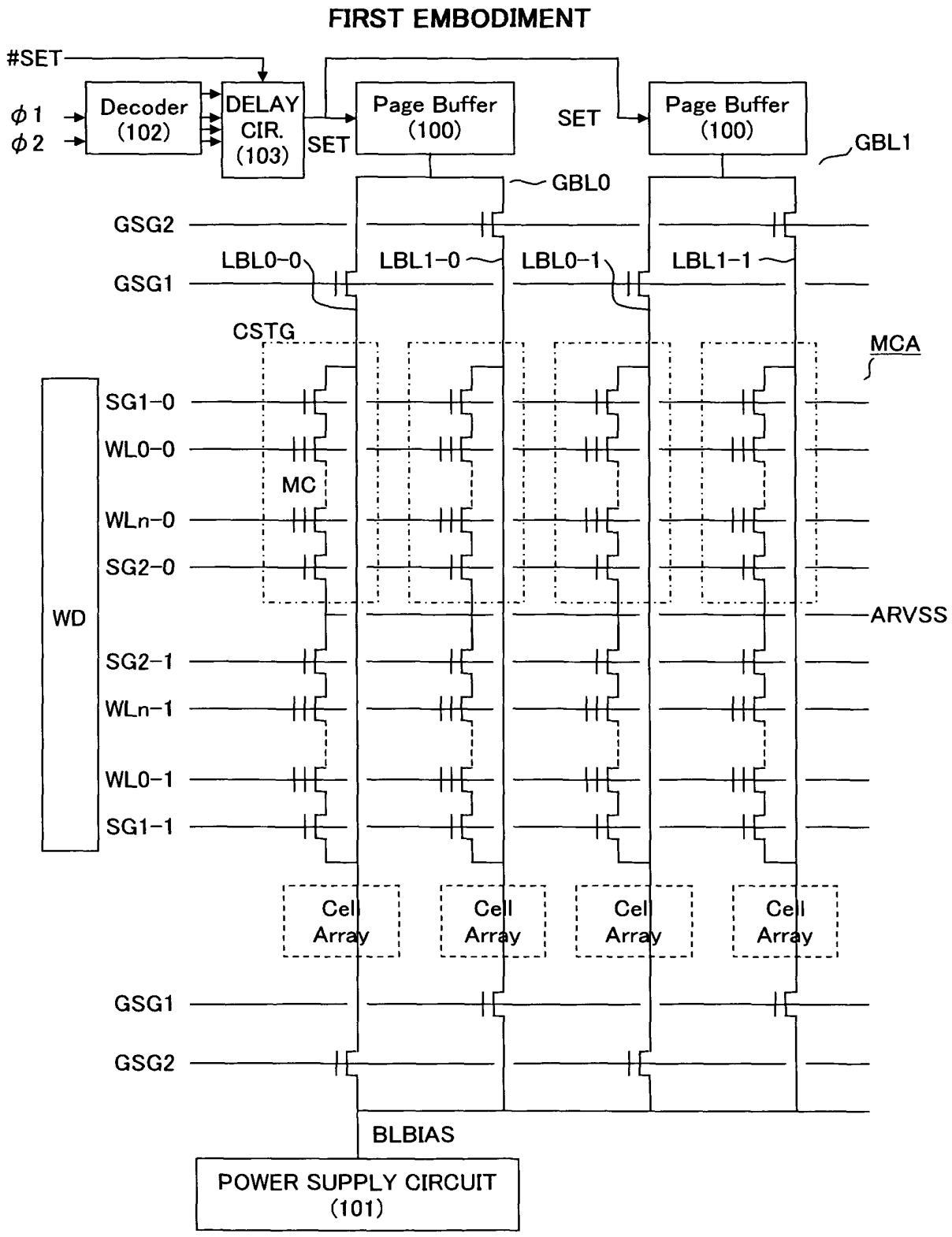

FIRST EMBODIMENT
#SET
φ1
φ2
Decoder (102)
DELAY CIR. (103)
SET
Page Buffer (100)
SET
Page Buffer (100)
GBL1
GBL0
GSG2
GSG1
LBL0-0
LBL1-0
LBL0-1
LBL1-1
CSTG
MCA
SG1-0
WL0-0
MC
WLn-0
SG2-0
WD
ARVSS
SG2-1
WLn-1
WL0-1
SG1-1
Cell Array
Cell Array
Cell Array
Cell Array
GSG1
GSG2
BLBIAS
POWER SUPPLY CIRCUIT (101)

FIG. 7

FIRST EMBODIMENT

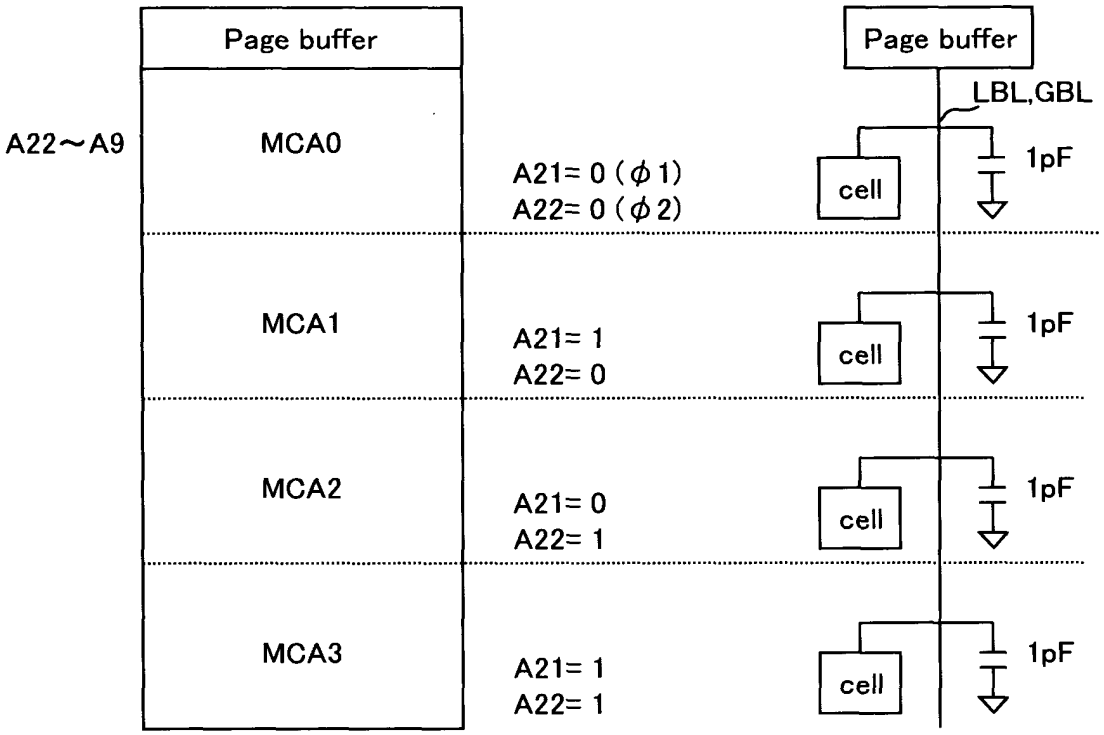


FIG. 8

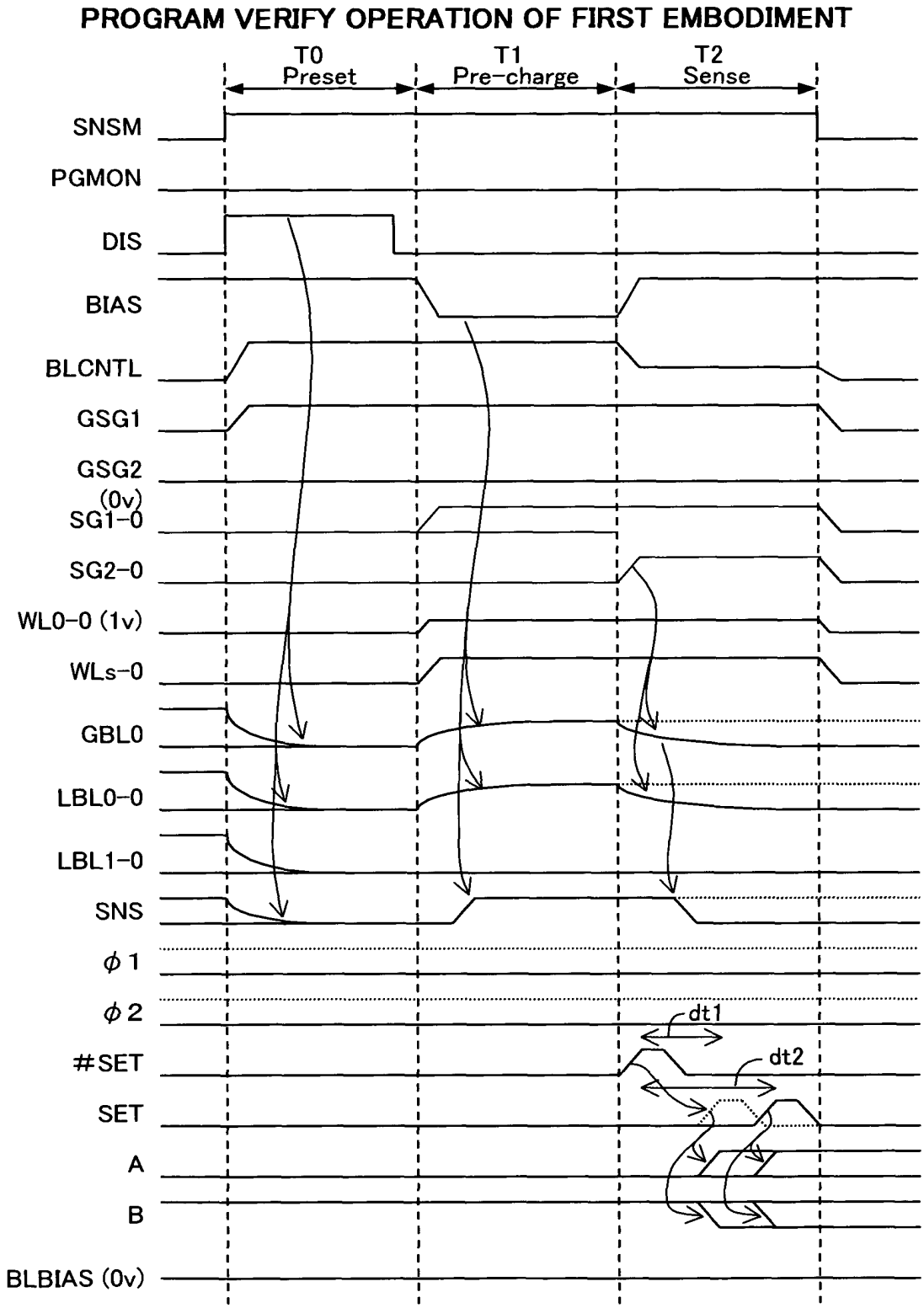

PROGRAM VERIFY OPERATION OF FIRST EMBODIMENT
T0
Preset
T1
Pre-charge
T2
Sense
SNSM
PGMON
DIS
BIAS
BLCNTL
GSG1
GSG2
(0v)
SG1-0
SG2-0
WL0-0 (1v)
WLs-0
GBL0
LBL0-0
LBL1-0
SNS
ϕ1
ϕ2
#SET
SET
A
B
BLBIAS (0v)
dt1
dt2

FIG. 9

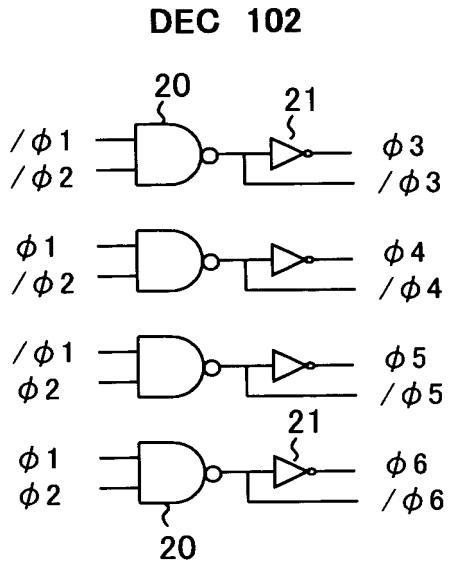

DEC 102
20
21
/φ1
/φ2
φ3
/φ3
φ1
/φ2
φ4
/φ4
/φ1
φ2
φ5
/φ5
21
φ1
φ2
φ6
/φ6
20

FIG. 10

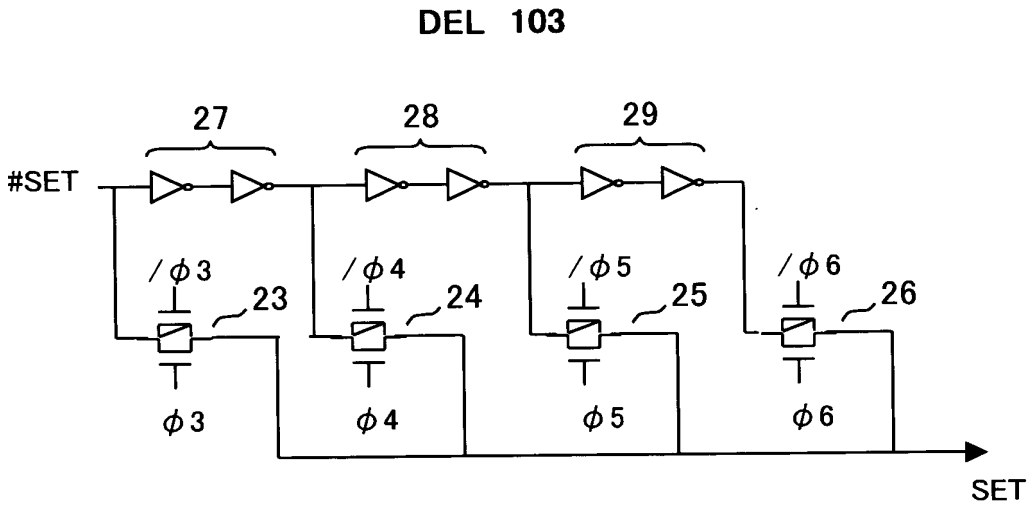

DEL 103
27
28
29
#SET
/φ3
/φ4
/φ5
/φ6
23
24
25
26
φ3
φ4
φ5
φ6
SET

FIG. 11

MODIFICATION (1) OF FIRST EMBODIMENT

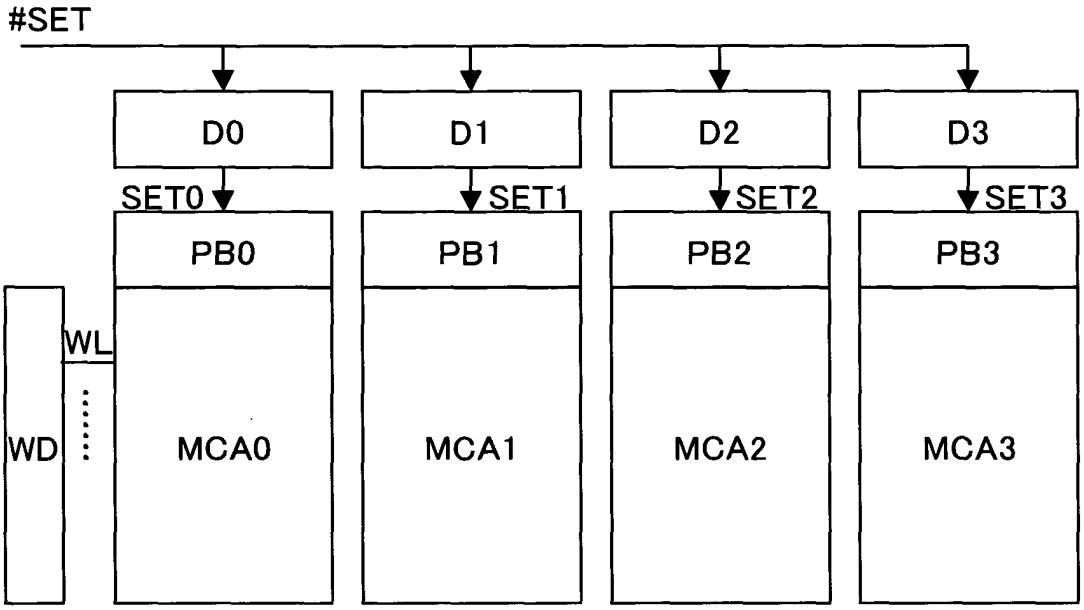


FIG. 12

MODIFICATION (2) OF FIRST EMBODIMENT

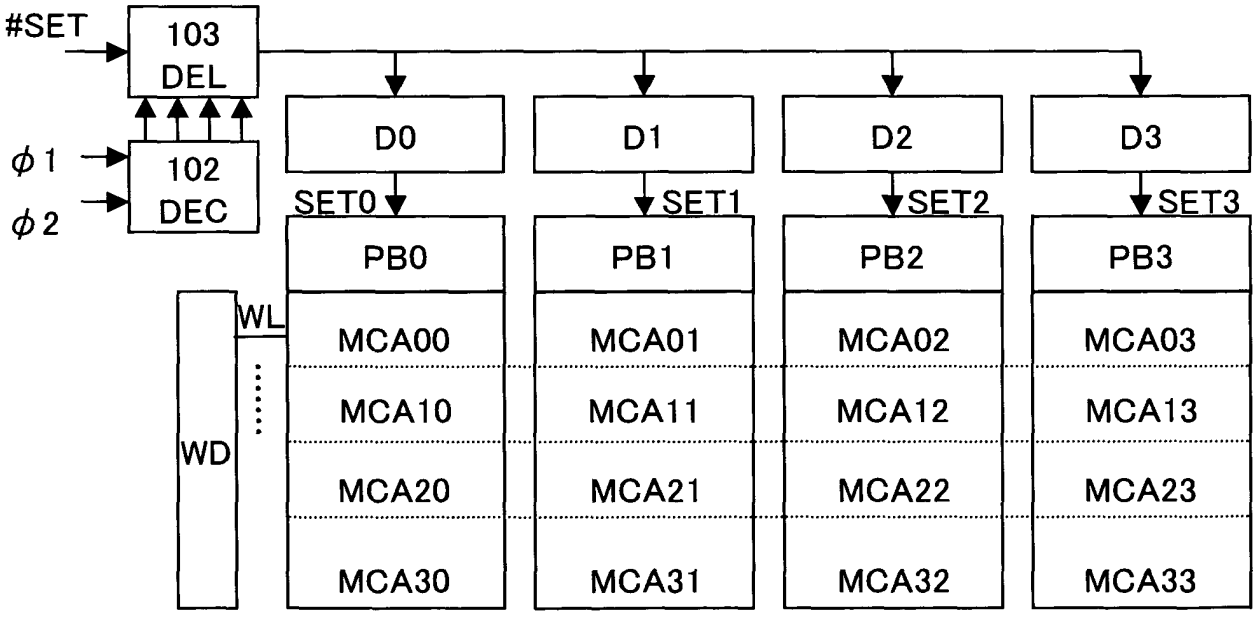


FIG. 13

SECOND EMBODIMENT

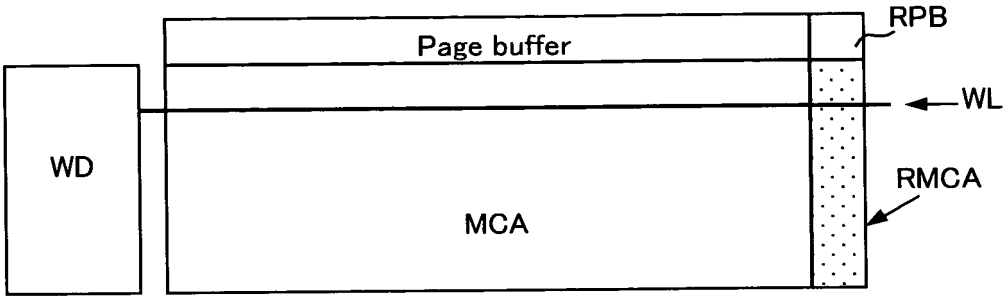


FIG. 14

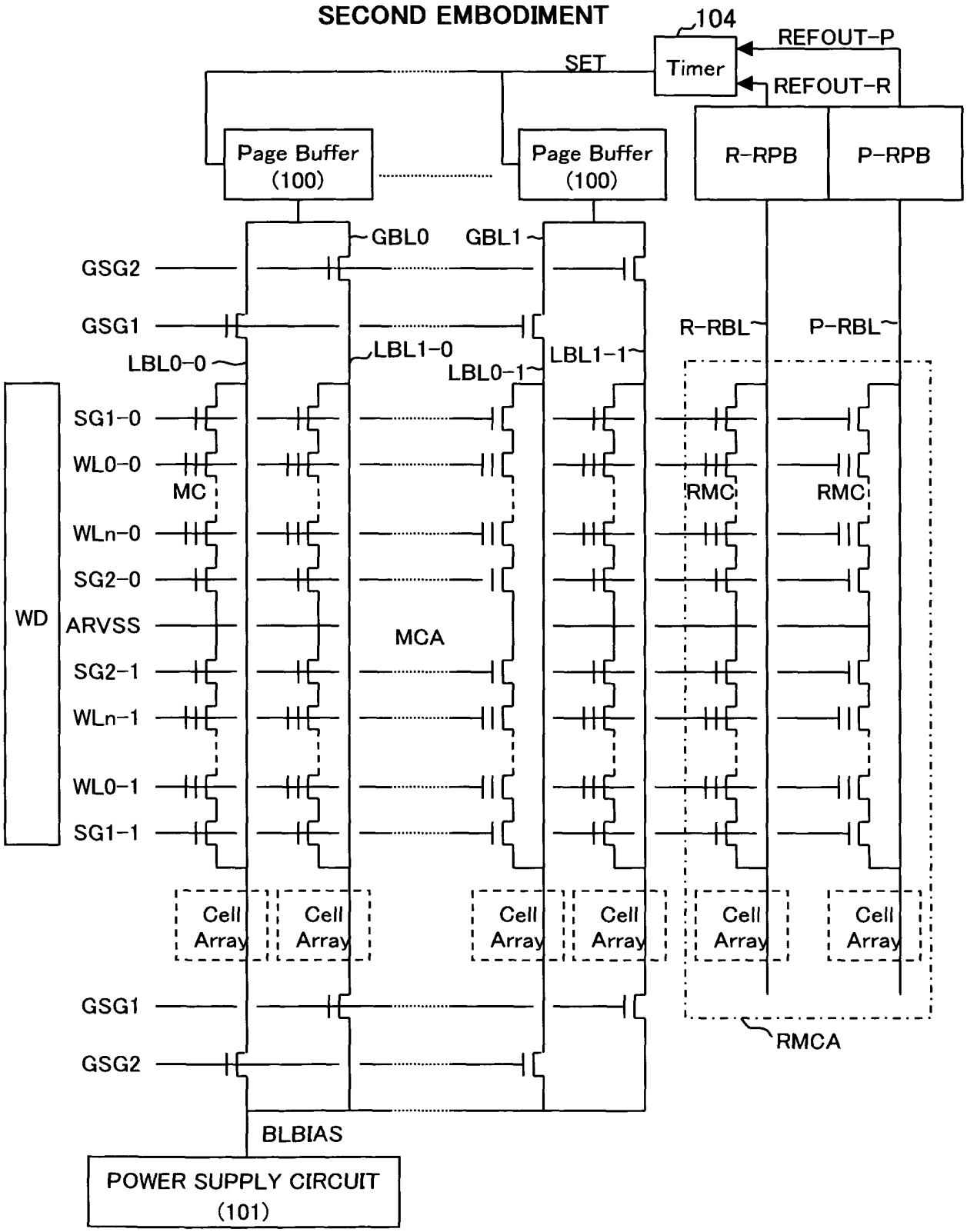

SECOND EMBODIMENT
104
Timer
SET
REFOUT-P
REFOUT-R
Page Buffer (100)
Page Buffer (100)
R-RPB
P-RPB
GBL0
GBL1
GSG2
GSG1
R-RBL
P-RBL
LBL0-0
LBL1-0
LBL0-1
LBL1-1
SG1-0
WL0-0
MC
RMC
RMC
WLn-0
SG2-0
WD
ARVSS
MCA
SG2-1
WLn-1
WL0-1
SG1-1
Cell Array
Cell Array
Cell Array
Cell Array
Cell Array
Cell Array
GSG1
GSG2
RMCA
BLBIAS
POWER SUPPLY CIRCUIT (101)

FIG. 15

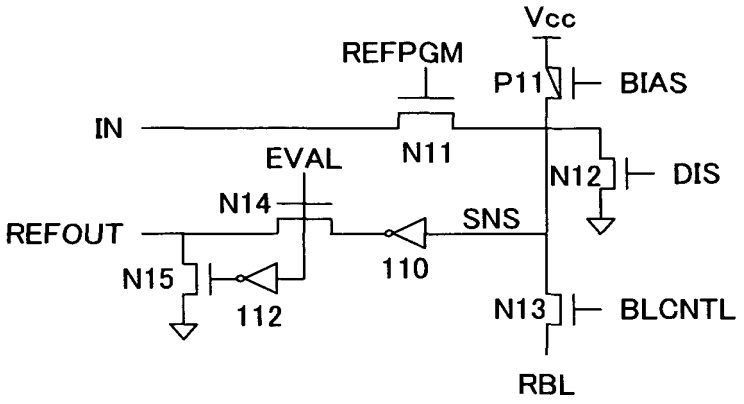

RPB
Vcc
REFPGM
P11
BIAS
IN
N11
EVAL
N12
DIS
N14
SNS
REFOUT
110
N15
112
N13
BLCNTL
RBL

FIG. 16

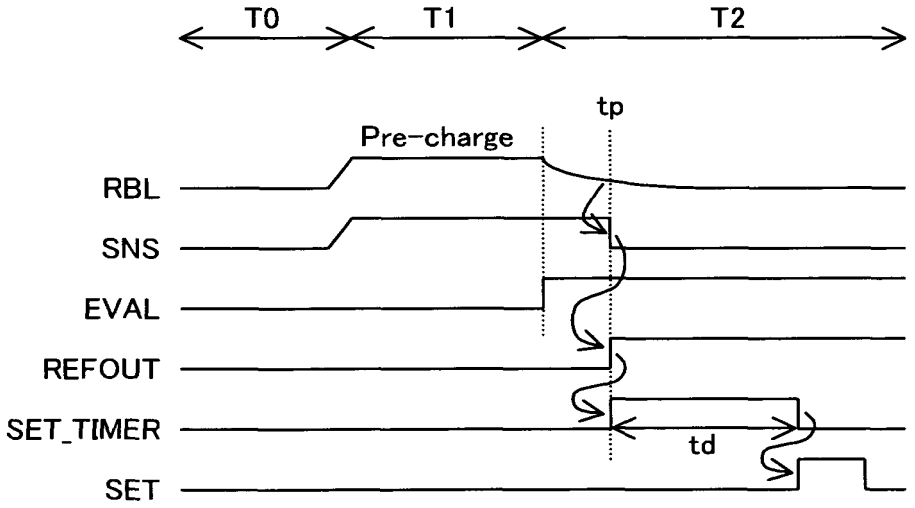

T0
T1
T2
tp
Pre-charge
RBL
SNS
EVAL
REFOUT
SET_TIMER
td
SET

FIG. 17

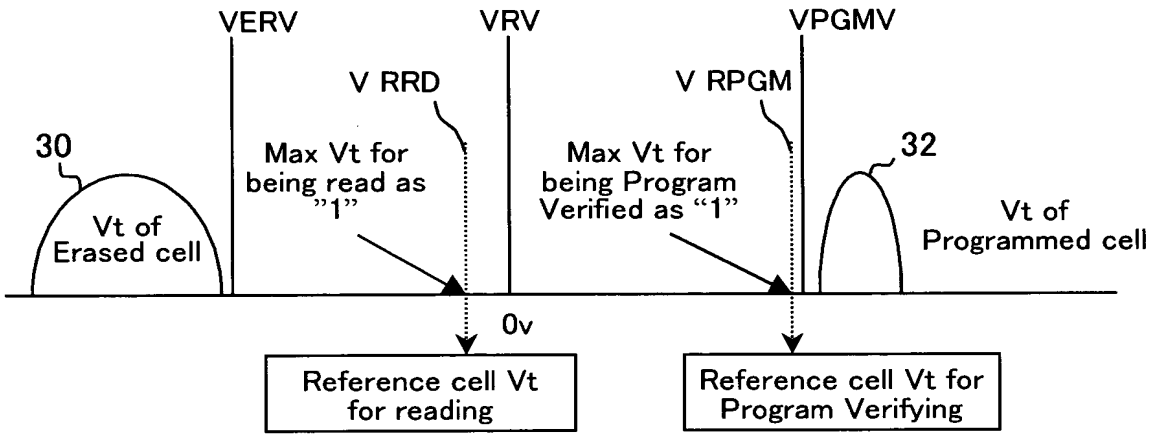

VERV
VRV
VPGMV
V RRD
V RPGM
30
32
Max Vt for being read as "1"
Max Vt for being Program Verified as "1"
Vt of Erased cell
Vt of Programmed cell
0v
Reference cell Vt for reading
Reference cell Vt for Program Verifying

FIG. 18

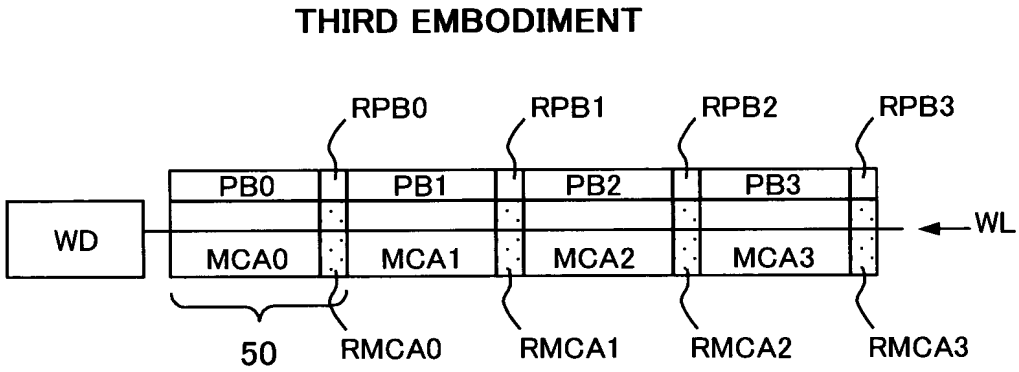

THIRD EMBODIMENT
RPB0
RPB1
RPB2
RPB3
PB0
PB1
PB2
PB3
WD
WL
MCA0
MCA1
MCA2
MCA3
50
RMCA0
RMCA1
RMCA2
RMCA3

FIG. 19

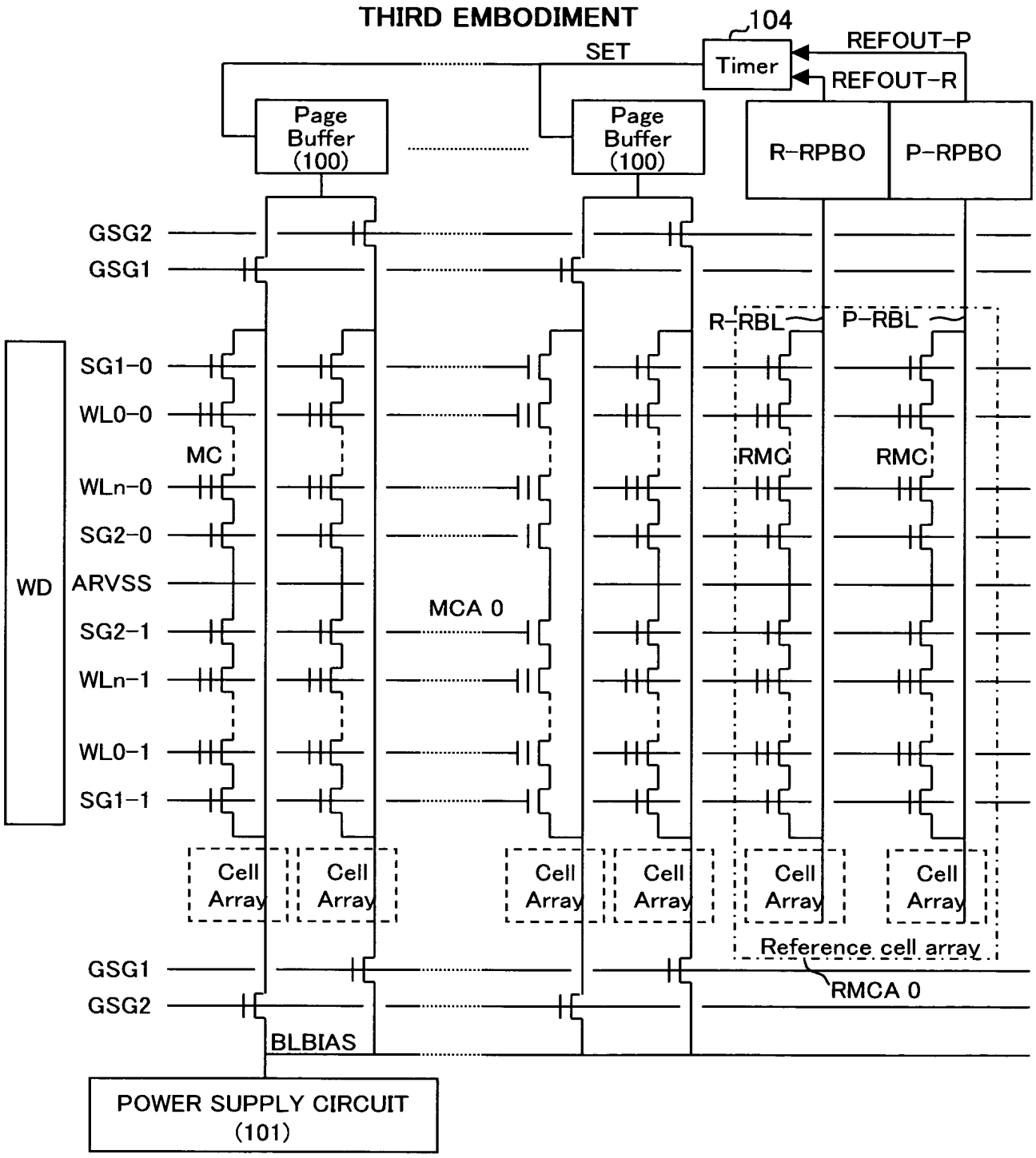
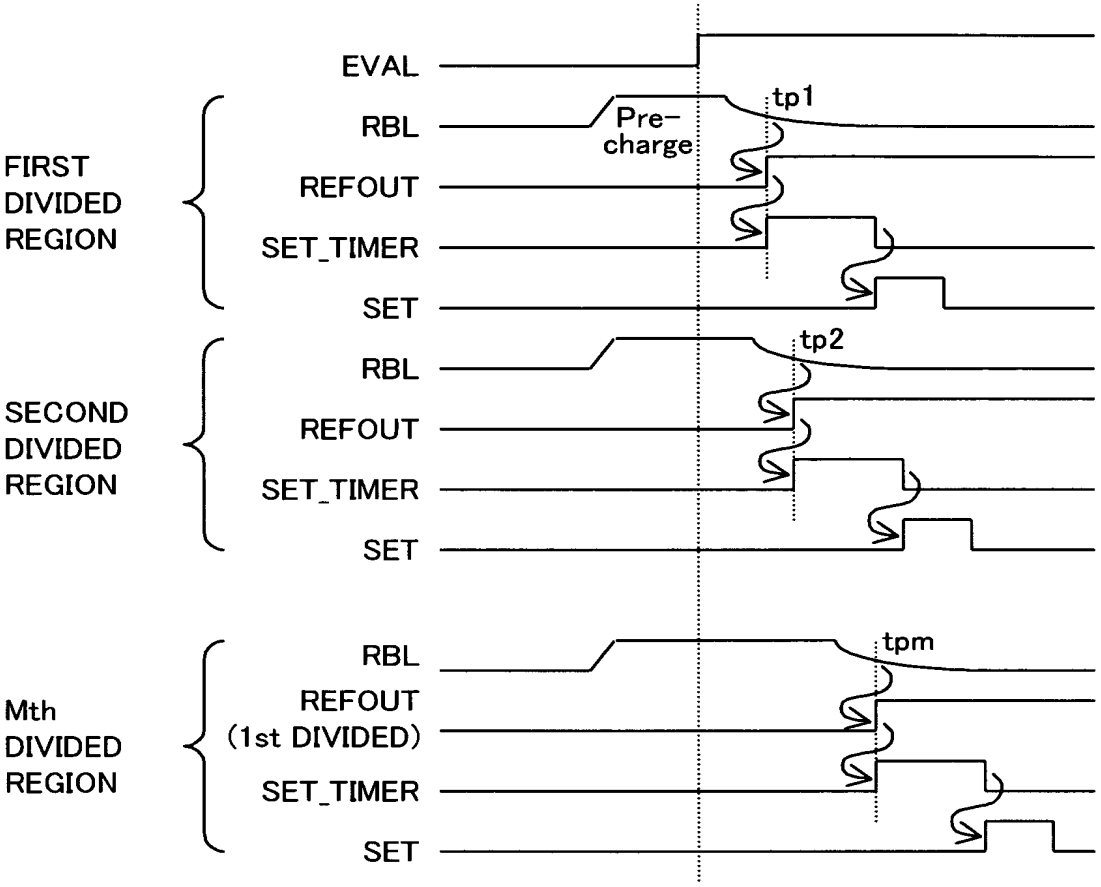

THIRD EMBODIMENT
104
Timer
SET
REFOUT-P
REFOUT-R
Page Buffer (100)
Page Buffer (100)
R-RPBO
P-RPBO
GSG2
GSG1
R-RBL
P-RBL
SG1-0
WL0-0
MC
RMC
RMC
WLn-0
SG2-0
WD
ARVSS
MCA 0
SG2-1
WLn-1
WL0-1
SG1-1
Cell Array
Cell Array
Cell Array
Cell Array
Cell Array
Cell Array
Reference cell array
GSG1
RMCA 0
GSG2
BLBIAS
POWER SUPPLY CIRCUIT (101)

FIG. 20


EVAL
RBL
Pre-
charge
tp1
REFOUT
SET_TIMER
SET
FIRST
DIVIDED
REGION
RBL
tp2
REFOUT
SET_TIMER
SET
SECOND
DIVIDED
REGION
RBL
tpm
REFOUT
(1st DIVIDED)
SET_TIMER
SET
Mth
DIVIDED
REGION